HASH IP Core

Introduction

This is a high performance, small footprint HASH IP Core. It supports three HASH algorithms: MD5, SHA1, SHA256. A S/G DMA engine keeps the core running. Each hash engine has it's own dedicated clock, which is independent of the main AXI clock.

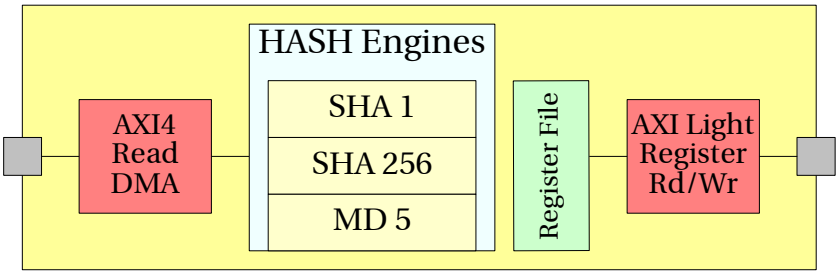
Features

The AES Crypt IP Core includes the following features:

- *Supports MD5, SHA1 and SHA256*
- *High Performance S/G DMA engine*
- *Fully AXI-4 compatible*
- *AXI-Light for register Interface*
- *Separate clocks for MD5, SHA and SHA256 engines and AXI interface*

Architecture

The HASH IP Core performs 3 different HASH calculation. Witch HASH is to b e used is determined in the CSR register. Once a starting TD address has been set, the DMA engine can be enabled. It will process TDs until it encounters a TD with the NEXT field of zero.



Size And Speed

Sample Synthesis results for HASH IP Core. The goal was smallest and fastest implementation.

Technology	*Gate Count*	*Fmax*
Virtex UltraScale+ Virtex UltraScale Kintex 7, Virtes 7	5,600 LUTs, 6,400 Registers 3 BRAMs	AXI Interface: >200 MHz Engines: >300 MHz
This IP Core can be implemented in any technology. There are no special/dedicated FPGA (or other) components in this IP Core.		

These synthesis results are provided for reference only.