

### ATA-7 Device IP Core

#### INTRODUCTION

This is a ATA-7 compliant device interface core used for interfacing custom devices to IDE controller. Core is targeted for SOC implementations in ASIC and FPGA.

#### FEATURES

Features supported are:

- PIO modes 0-4
- IORDY signaling for PIO cycle extension
- Multi-word DMA modes 0-2
- Ultra DMA modes 0-6
- Programmable timings for PIO and DMA modes
- Support for Ultra DMA pause and termination
- Standard slave Wishbone interface to microprocessor/microcontroller

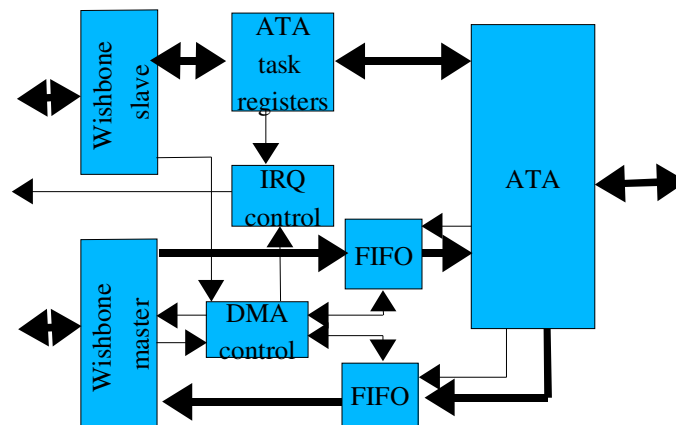
- Interrupt generator for IRQ driven software driver implementation
- Automatic handling of BSY and DRQ bits
- DMA engine and master Wishbone interface for data transfer
- Small register FIFOs for transmit and receive data
- Acts as a single, master ATA/ATAPI device on ATA cable
- 66MHz clock for UDMA133 (mode 6) operation

Additional functions or customization can be easily done per customers request.

ATA device core is written in Verilog.

#### ARCHITECTURE

ATA device core architecture with its main sub blocks is shown on a figure bellow.



### VERIFICATION

ATA device core has been thoroughly exercised. A self checking Verilog test bench with a test suite is supplied with the core. Test suit includes all major modes of core operation : configuration, PIO transfers, multi-word DMA, Ultra DMA with examples of device and host terminating/pausing data-in/data-out bursts.

ATA device core demo is available, demonstrating core usage in Xilinx MicroBlaze base SOC implemented on Xilinx Virtex V4LX25LC. Demo is a fully functional ATA7 hard drive that can be connected to PC IDE controller.

### SIZE AND SPEED

Sample Synthesis results. The goal was smallest and fastest implementation.

<i>Technology</i>	<i>Gate Count</i>	<i>Operating Frequency</i>
Xilinx Virtex 2	1100 LUTs	> 66MHz
UMC 0.18	4.8K	> 66MHz

These synthesis results are provided for *reference only*. Please contact us for estimates for your application.

All ASICS World Services, LTD. IP Cores now support the following buses:

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